REMARKS

Claims 10 and 16 are cancelled. Claims 7 and 13 are amended herein. No new matter is introduced as a result of the Claim amendments.

35 U.S.C. § 102 Rejections

Claims 13-14 are rejected under 35 U.S.C. § 102 (e) as being anticipated by the Tuan et. al, (U.S. Patent No. 6,617,636), hereinafter referred to as "Tuan." Claim 13 is amended herein and recites:

> A method for fabricating a memory device comprising:
> depositing a plurality of layers upon a semiconductor substrate;
> patterning said plurality of layers to create a stack gate; and
> performing a rapid thermal oxidation (RTO) upon said stack gate, wherein additional oxide material is created in a damaged region of an oxide layer of said stack gate.

The Applicants respectfully submit that the cited reference of Tuan does not teach or suggest creating additional oxide material in a damaged region of an oxide layer of a stack gate as a result of a rapid thermal oxidation process. Thus, the Applicants respectfully submit that the present invention, as recited in independent Claim 13 traverses the Examiner's objection under 35 U.S.C. § 102 (e) as being anticipated by Tuan.

Claims 14 depends from Claim 13 and recites additional limitations descriptive of embodiments of the present invention. Therefore, the Applicants respectfully submit that Claim 13 also overcomes the Examiners rejection under 35 U.S.C. § 102 (e).

35 U.S.C. § 103 Rejections

Claims 1-18 are rejected under 35 U.S.C. § 103 (a) as being unpatentable over Nitta (U. S. Patent No. 6,582,998), hereinafter referred to as "Nitta," in view of Fujishiro et. al (U. S. Patent No. 5,294,571), hereinafter referred to as "Fujishiro." Claim 1 recites:

> fabricating a gate structure comprising a tunnel oxide layer, a floating gate layer, an oxide layer, and a control gate layer on a semiconductor substrate; and
>
> repairing said tunnel oxide layer using a rapid thermal oxidation (RTO) process.

Claims 7 and 13 recite similar claim limitations with the added limitation that additional oxide material is created in a damaged region of a gate structure of the memory device. The Applicants respectfully submit that Nitta does not teach or suggest the claim limitations recited in Claims 1, 7, and 13 of the present invention. Furthermore, Nitta does not teach that the tunnel oxide layer is in any manner damaged during the process to fabricate the gate structure upon the substrate. Also, there is no suggestion that the deposition method of Nitta can be used to repair the damage to the tunnel oxide layer which extends beneath the floating gate layer of the gate structure. Accordingly, the Applicants respectfully submit that the problem of damage to the tunnel oxide layer as a result of etching the stack gate is neither identified nor remedied based upon the teaching of Nitta.

The Applicants respectfully submit that Fujishiro fails to overcome the shortcomings of Nitta. For example, Fujishiro merely teaches forming a SiO2 layer upon a substrate. However, Fujishiro does not teach or suggest that the problem of damage of the tunnel oxide layer occurs as a result of fabricating the gate structure. Additionally, there is no suggestion that the fabrication method of Fujishiro can be used to repair the damage to the tunnel oxide layer which extends beneath the floating gate layer of the gate structure. Furthermore, Fujishiro does not teach or suggest repairing a tunnel oxide layer damaged as a result of fabricating a gate structure of a flash memory device.

Additionally, the Applicants respectfully submit that the determination of obviousness cannot be based on the hindsight combination of components selectively culled from the prior art to fit the parameters of the present invention. There must be a teaching or suggestion within the prior art to select particular elements, and to combine them in the way claimed. The Applicants respectfully submit that neither Nitta nor Fujishiro teach or suggest that the tunnel oxide layer of a flash memory is damaged as a result of fabricating the gate structure of the flash memory device, nor do they teach or suggest a method for repairing it. Therefore, a combination of Nitta and Fujishiro to repair a damaged tunnel oxide layer as recited in the present invention is not suggested. Accordingly, the Applicants respectfully submit that the objections to Claims 1, 7, and 13 under 35 U.S.C. § 103 (a) are overcome.

Claims 2-6 depend from Claim 1 and recite additional claim limitations descriptive of embodiments of the present invention. Accordingly, the Applicants respectfully submit that the objections to Claims 2-6 under 35 U.S.C. § 103 (a) are overcome.

Claims 8-9 and 11-12 depend from Claim 7 and recite additional claim limitations descriptive of embodiments of the present invention. Accordingly, the Applicants respectfully submit that the objections to Claims 8-9 and 11-12 under 35 U.S.C. § 103 (a) are overcome.

Claims 14-15 and 17-18 depend from Claim 13 and recite additional claim limitations descriptive of embodiments of the present invention. Accordingly, the Applicants respectfully submit that the objections to Claims 14-15 and 17-18 under 35 U.S.C. § 103 (a) are overcome.

CONCLUSION

In light of the above remarks, the Applicants respectfully request reconsideration of the rejected Claims.

Based on the arguments presented above, the Applicants respectfully assert that Claims 1-9, 11-15, and 17-18 overcome the rejections of record and, therefore, the Applicants respectfully solicit allowance of these Claims.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

WAGNER, MURABITO & HAO LLP

Date: Aug. 24, 2004

Anthony C. Murabito
Reg. No. 35,295

Two North Market Street
Third Floor
San Jose, California 95113
(408) 938-9060